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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,051	03/12/2001	Salman Akram	MIO 0069 PA	7513

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EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,051	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6-8,25-36,47,49-51,53-58 and 60-62* is/are pending in the application.

4a) Of the above claim(s) *58 and 60-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6-8,25-36,47,49-51 and 53-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the request for continued examination filed November 19, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 8 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (U.S. 6,300,163) in combination with Watanabe et al. (U.S. 2002/0074669), Kweon et al. (U.S. 5,656,856 and Suzuki et al (US 5,532,910).

Akram (Fig 3) discloses a multiple die semiconductor assembly comprising: a first semiconductor die (32) having a first active surface, said first active surface including at least one conductive bond pad (not labeled; connected to wire); a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad; an intermediate substrate (12) positioned between said first active surface (top portion) of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate (bottom) faces said first active surface and such that a second surface (top portion) of said intermediate substrate faces said second active surface (bottom portion), wherein said intermediate substrate includes a net-work of conductive contact (PCB comprises contacts on a dielectric material) , said first

semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact (i.e. wires , 31) extending from said first active surface to said first surface of said intermediate substrate, and said second semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact (37) extending from said second active surface to said second surface of said intermediate substrate.

Akram does not disclose at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die , said second semiconductor die, or a topographic contact .

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48), but does not illustrate the various locations that capacitors can be placed in a package.

Watanabe (Fig 4-6) and Kweon et al. (Fig 1) discloses examples of capacitors conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in the package of Akram, such the capacitor coupled to a die and is accommodated in various spaces defined by a thickness dimension as illustrated by Watanabe and Kweon in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

Furthermore, the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Claim 7, 49-51, 54 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (U.S. 2002/0079573) in combination with Watanabe et al. (U.S. 2002/0074669), Kweon et al. (U.S. 5,656,856) and Suzuki et al (US 5,532,910).

Akram '573 (Fig 3) discloses a multiple die semiconductor assembly comprising: a first semiconductor die (12) defining a first active surface (portion in contact with wire; not labeled), said first active surface including at least one conductive bond pad (i.e. portion along die connected to wire; not labeled); a second semiconductor die (212) defining a second active surface (portion in contact with wire; not labeled), said second active surface including at least one conductive bond pad (not shown); an intermediate substrate (214) positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface (i.e. bottom portion) of

said intermediate substrate faces said first active surface and such that a second surface (i.e. top portion) of said intermediate substrate faces said second semiconductor die, wherein said intermediate substrate-includes a network of conductive contacts formed thereon (i.e. PCB), said intermediate substrate defines a passage (not labeled) there through, said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line (18; wire) extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate; and an additional substrate (214) positioned such that a first surface (i.e. bottom portion) of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate, wherein said additional substrate includes a network of conductive contacts formed thereon (i.e. boards with contacts, not labeled, connected to wires), said additional substrate define an additional passage there through, said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line (wire; not labeled) extending from said conductive bond pad of said second semiconductor die through said

additional passage defined in said additional substrate and to a conductive contact (i.e. contacts on board in COB configuration) on a second surface of said additional substrate and a third intermediate substrate (214; i.e. above the other substrates), positioned such that first surface (bottom portion; alternatively the top portion) of the third substrate faces said second surface of the additional substrate with the intermediate substrate electrically coupled by at least one topographic contact extending form said second surface of the third substrate to the first surface of the intermediate substrate(i.e. item 132, 232) to the third substrate, but does not appear to disclose at least one decoupling capacitor decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

Akram does not appear to disclose at least one decoupling capacitor decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

Watanabe (Fig 4-6) and Kweon (Fig 1) discloses capacitors conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48).

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in the package of Akram, such the capacitor coupled to a die and is accommodated in a various spaces defined by a thickness dimension as illustrated by Watanabe and Kweon in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

Furthermore, the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Claims 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (U.S. 2002/0079573), Watanabe (U.S. 2002/0074669) and Kweon et al. (U.S.

5,656,856) and Suzuki et al (US 5,532,910) as applied to claim 7 and further in combination with Spielberger et al. (U.S. 6,005,778).

Neither Akram, Watanabe, Kweon nor Suzuki appears to show the use of a pair of capacitors.

Spielberger (Fig 5) utilizes a pair of capacitors.

It would have been obvious to one of ordinary skill in the art to incorporate a pair of capacitor to the modified package of Akram and Suzuki to further reduce propagation delays as taught by Spielberger (Col. 1, Lines 37-43).

Claims 2, 6, 25-36 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yenkateshwaran (US 6,388,336), Watanabe (U.S. 2002/0074669), Kweon et al. (U.S. 5,656,856) in combination with Suzuki et al (US 5,532,910).

Yenkateshwaran (Fig 2) a multiple die semiconductor assembly comprising: a first semiconductor die (21a; alternately the second die because 1st, 2nd are subjective relational terms that defined by the person viewing it) defining a first active surface including at least one conductive bond pad (21c); a second semiconductor die (25a; alternately the first die) defining a second active surface (25b), said second active surface including at least one conductive bond pad (not labeled connected to bump, 26); an intermediate substrate positioned between said first semiconductor and said second semiconductor die, such that a first surface (i.e. bottom surface; alternatively the top surface) of said intermediate substrate faces said first semiconductor die and such that a second surface (i.e. top portion; alternatively the bottom surface) of said

intermediate substrate faces said second semiconductor die, wherein said intermediate substrate defines a passage there through and one of said die is positioned such that said conductive bond pad (21c) on one of first and second active surfaces is aligned with passage; a first surface (bottom portion) of the intermediate substrate facing an active surface (in contact with pad 21c) and the second surface (top) of the substrate faces the second active surface of the second die (i.e. flip chip), 25a) with the conductive line (24) extending form said conductive pad of the second die through said passage defined in said intermediate substrate, and to contact on said first surface of said intermediate substrate; with 1st/2nd die comprising a flip chip (25a); with topographic contacts,(26) extending between inherent pads of active surface (i.e. underneath bump, 26; not labeled); with a first die comprises a stacked chip (21a) secured (23a) to the intermediate substrate; conductive lines (24, 26) extending from said conductive bond pads on said first active surface to conductive contacts on said second surface of said intermediate substrate; further discloses conductive bond pad (21c) on said second active surface is aligned with said passage; and said first semiconductor die is electrically coupled to said intermediate substrate and said second semiconductor die is electrically (items 26,24) coupled to said intermediate substrate; and said first semiconductor die is electrically coupled to said second semiconductor die(i.e. both dies connected to item 22a); wherein said first/second semiconductor die (21a) is electrically coupled to said intermediate substrate by at least one conductive line (24) extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to said second surface

of said intermediate substrate; said assembly further comprises an underfill/ encapsulant material (27) formed over said first surface of said intermediate substrate; said assembly further comprises an underfill material formed between said first semiconductor die and said first surface of said intermediate substrate; and an encapsulant (27) formed over said first semiconductor die and said first surface of said intermediate substrate and between said first semiconductor die and said first surface of said intermediate substrate; and an encapsulant (27) formed over said second semiconductor die (25a,21a); and a die attach adhesive (23a) positioned to secure said second semiconductor die to said second surface of said intermediate substrate.

Yenkateshwaran does not appear to show a decoupling capacitor conductively coupled to at least on of said first and second dies, wherein the thickness dimension of the capacitor is accommodated in a space defined by a thickness dimension of one of first and second die or topographic contact connected to a first or second die.

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die (Col. 1, Lines 48).

Watanabe (Fig 4-6) and Kweon et al. (Fig 1) discloses capacitors conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in the package of Yenkateshwaran, such the capacitor coupled to a die and is accommodated in various spaces defined by a thickness dimension as illustrated by Watanabe and Kweon in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

Furthermore, the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Claims 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yenkateshwaran (US 6,388,336), Watanabe (U.S. 2002/0074669), Kweon et al. (U.S. 5,656,856) and Suzuki et al (US 5,532,910) as applied to claim 6 and further in combination with Spielberger et al. (U.S. 6,005,778).

Neither Yenkateshwaran, Watanabe, Kweon nor Suzuki appears to show the use of a pair of capacitors.

Spielberger (Fig 5) utilizes a pair of capacitors.

It would have been obvious to one of ordinary skill in the art to incorporate a pair of capacitors to the modified package of Yenkateshwaran and Suzuki to further reduce propagation delays as taught by Spielberger (Col. 1, Lines 37-43).

Response to Arguments

Applicant's arguments filed November 19, 2004 have been fully considered, but are found unpersuasive.

Applicant's gravamen is based on two contentions. First applicant contends that the rearrangement increases density and therefore is not mere design choice, secondly that none of the prior art give guidance to placing the capacitor in the thickness areas claimed. Examiner respectfully disagrees.

Because the placement of components in certain ways are known to affect density as illustrated for example in Takemura (JP4030926266; English abstract), the fact that applicant merely rearranges its capacitors in various places within a package does not produce any new and unexpected result, applicant's arguments are found unpersuasive. Furthermore the fact that applicant's capacitors can be moved to different locations establishes that its placement is not critical to the operation of it device; therefore applicant arguments are deemed unpersuasive.

In regard to guidance, it is sufficient that a general disclosure suggesting the incorporation of a capacitor in a package such as shown for example in Uchida (U.S. 5,648,667) encompasses placement of that capacitor anywhere in the package. Furthermore guidance is also gleamed from the additional references cited which only provide a small example of countless embodiments that place capacitors in various places in packages. Most notably, Watanabe et al. (U.S. 2002/0074669), Kweon (U.S 5,656,856) and Ueda (U.S. 5,701,033) provide guidance for the placement of capacitors

in a thickness direction of contacts of a device, the electrical devices or contacts of interposer/substrates.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
February 4, 2004

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER